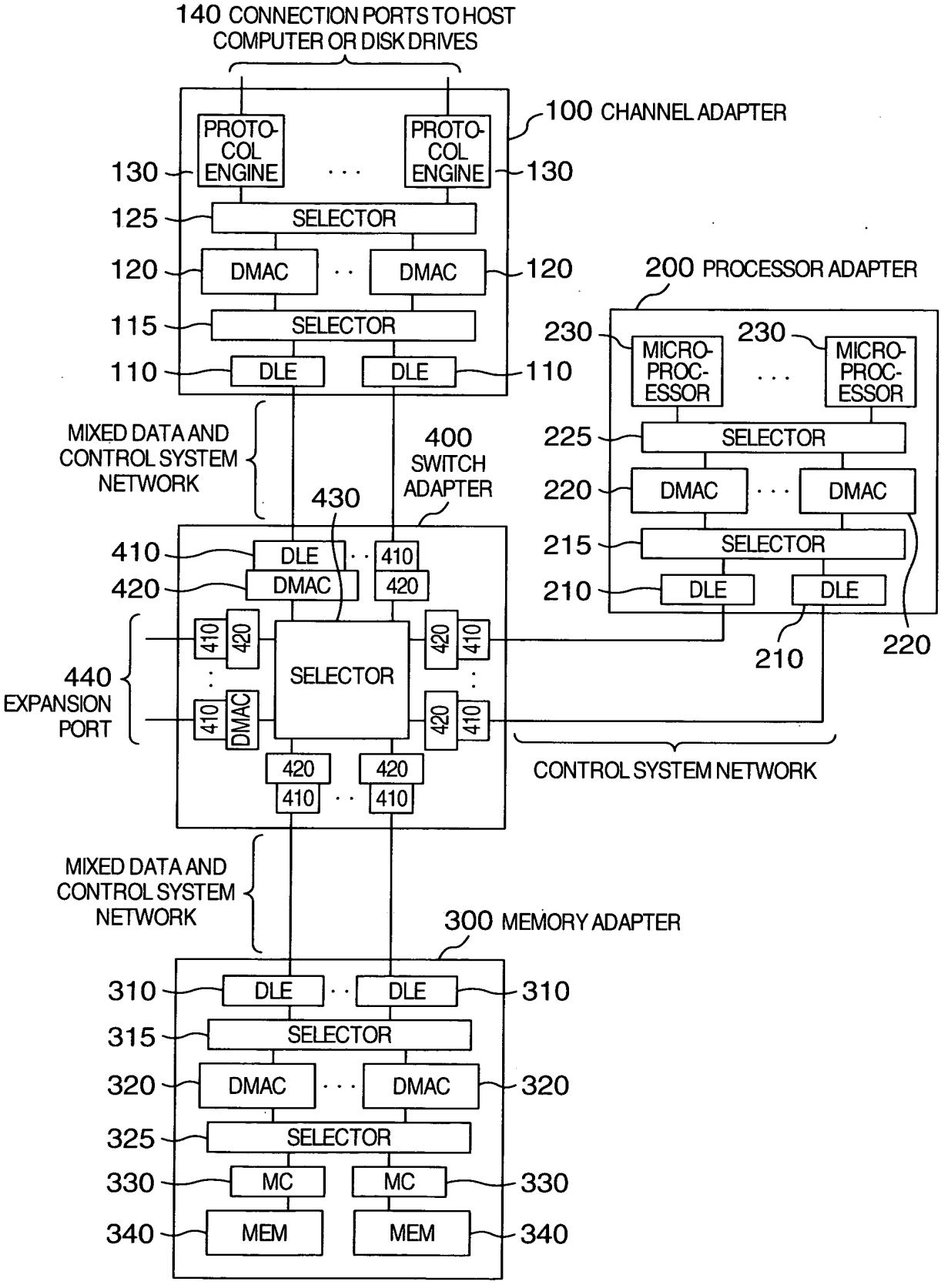
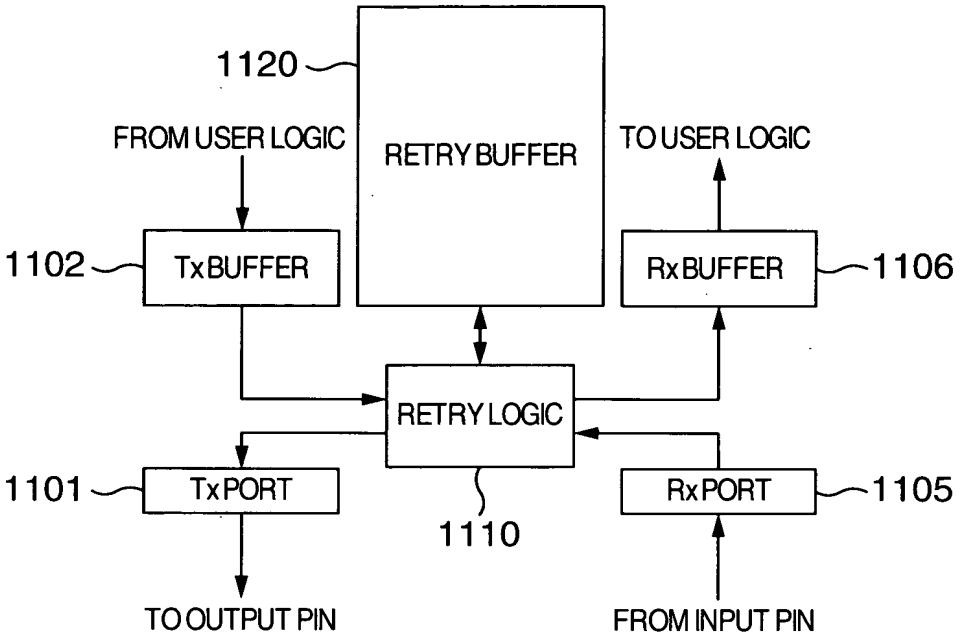
# FIG. 1



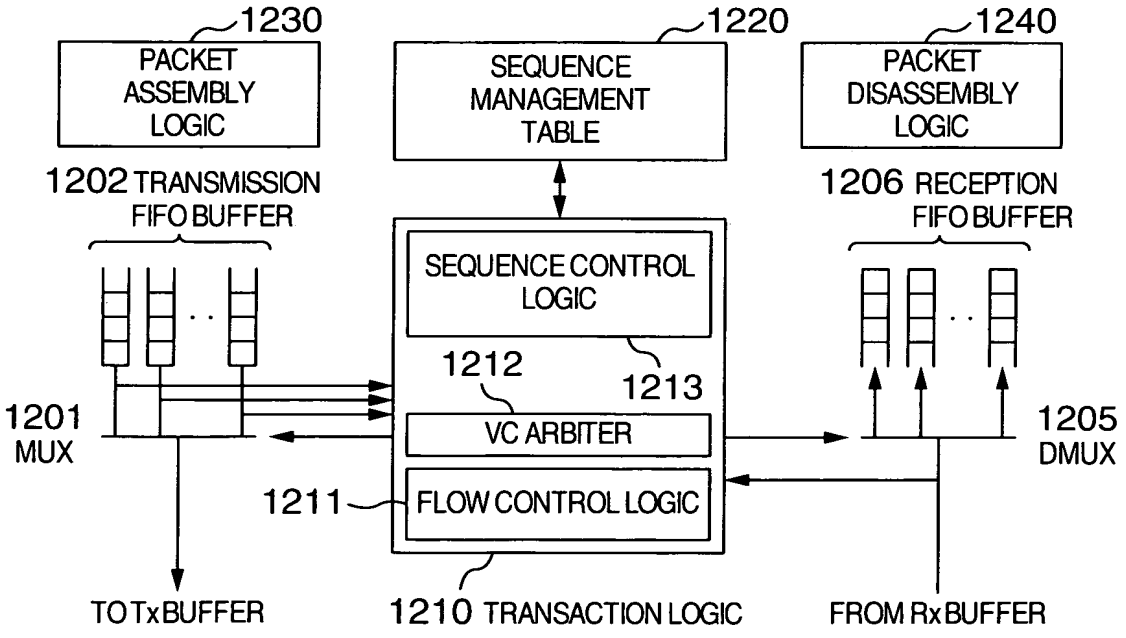

DISK CONTROLLER OF INVENTION

FIG. 2



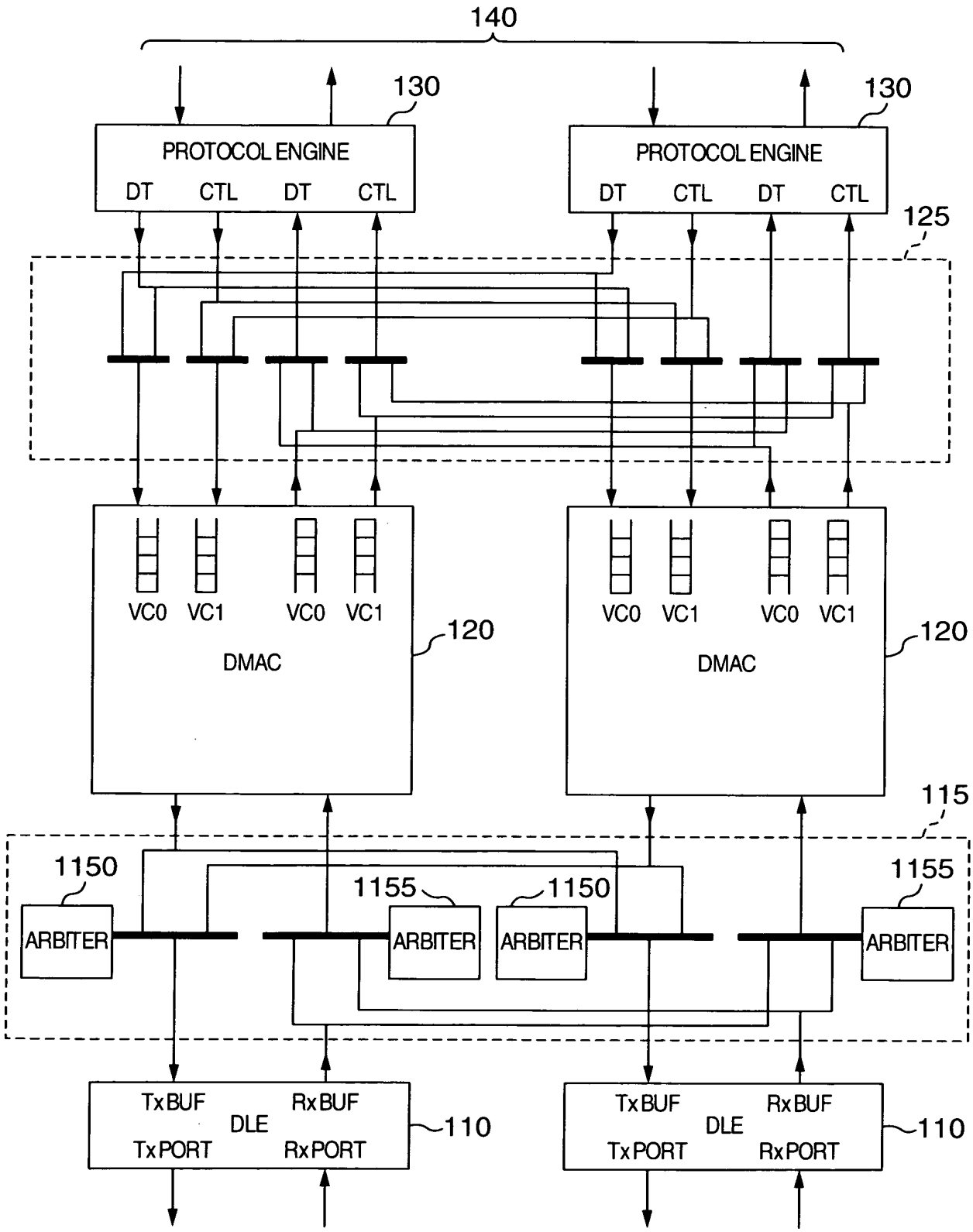

DLE STRUCTURE USED BY INVENTION

FIG. 3



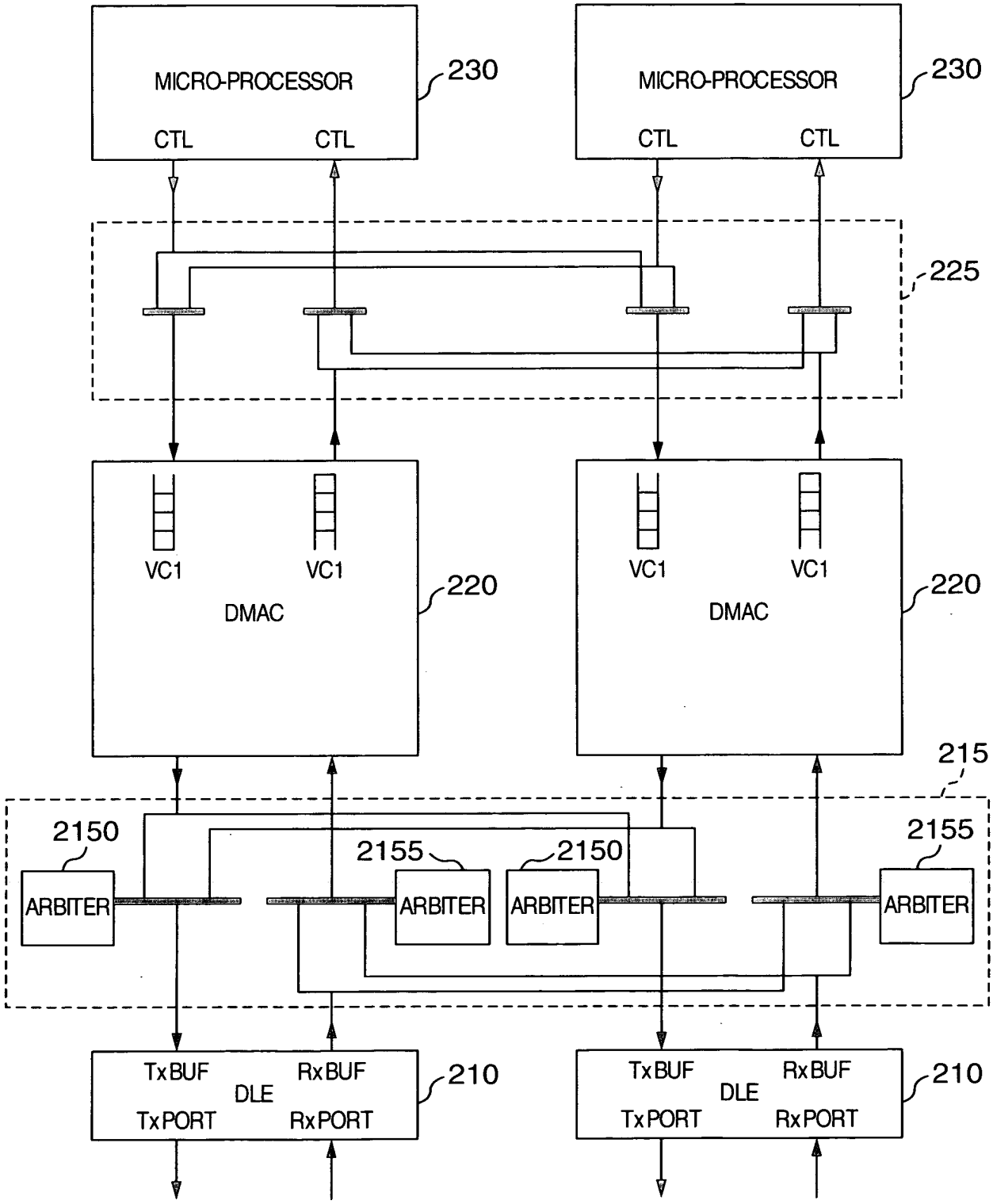

DMAC STRUCTURE USED BY INVENTION

# FIG. 4



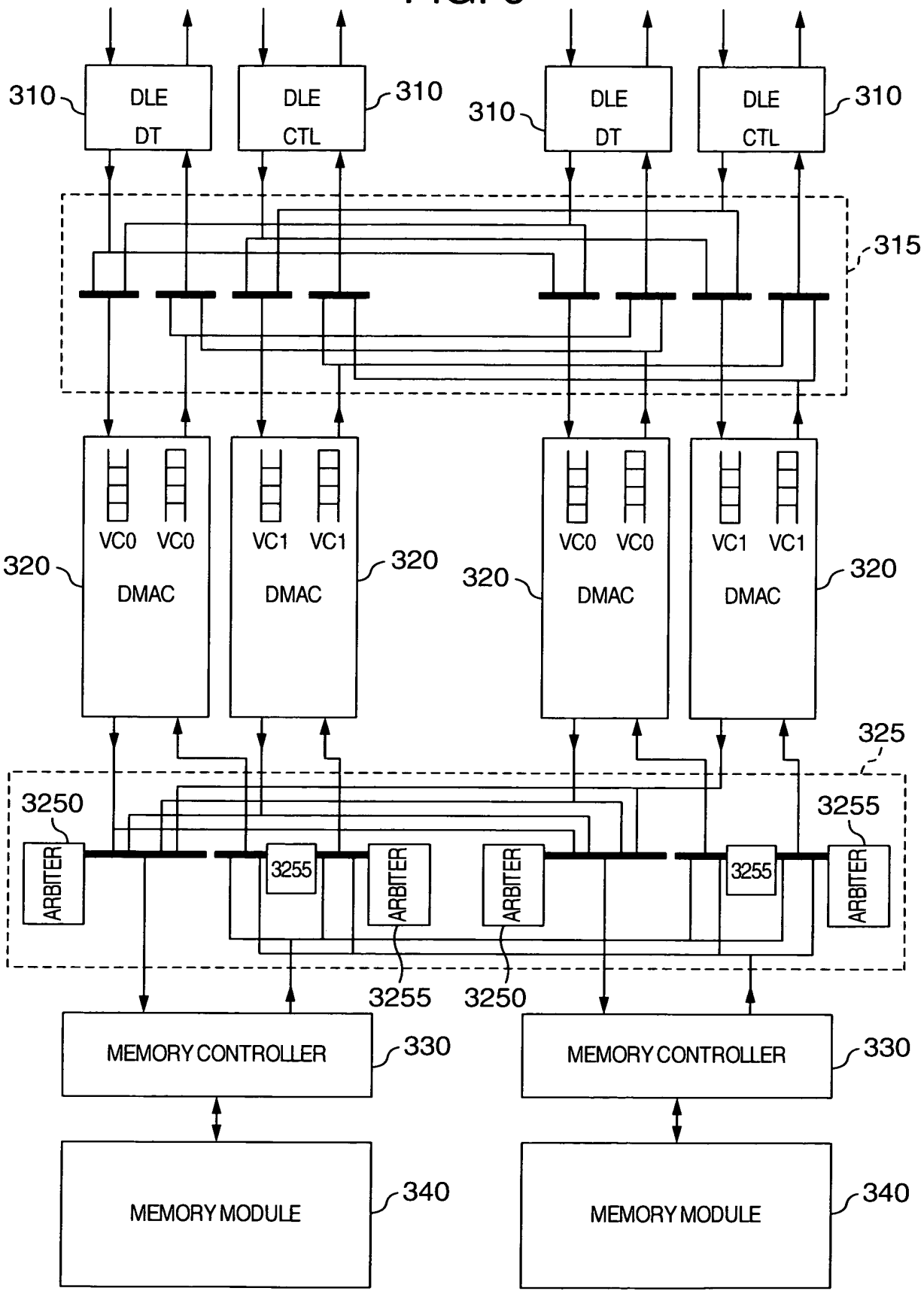

CHANNEL ADAPTER STRUCTURE USED BY INVENTION

FIG. 5



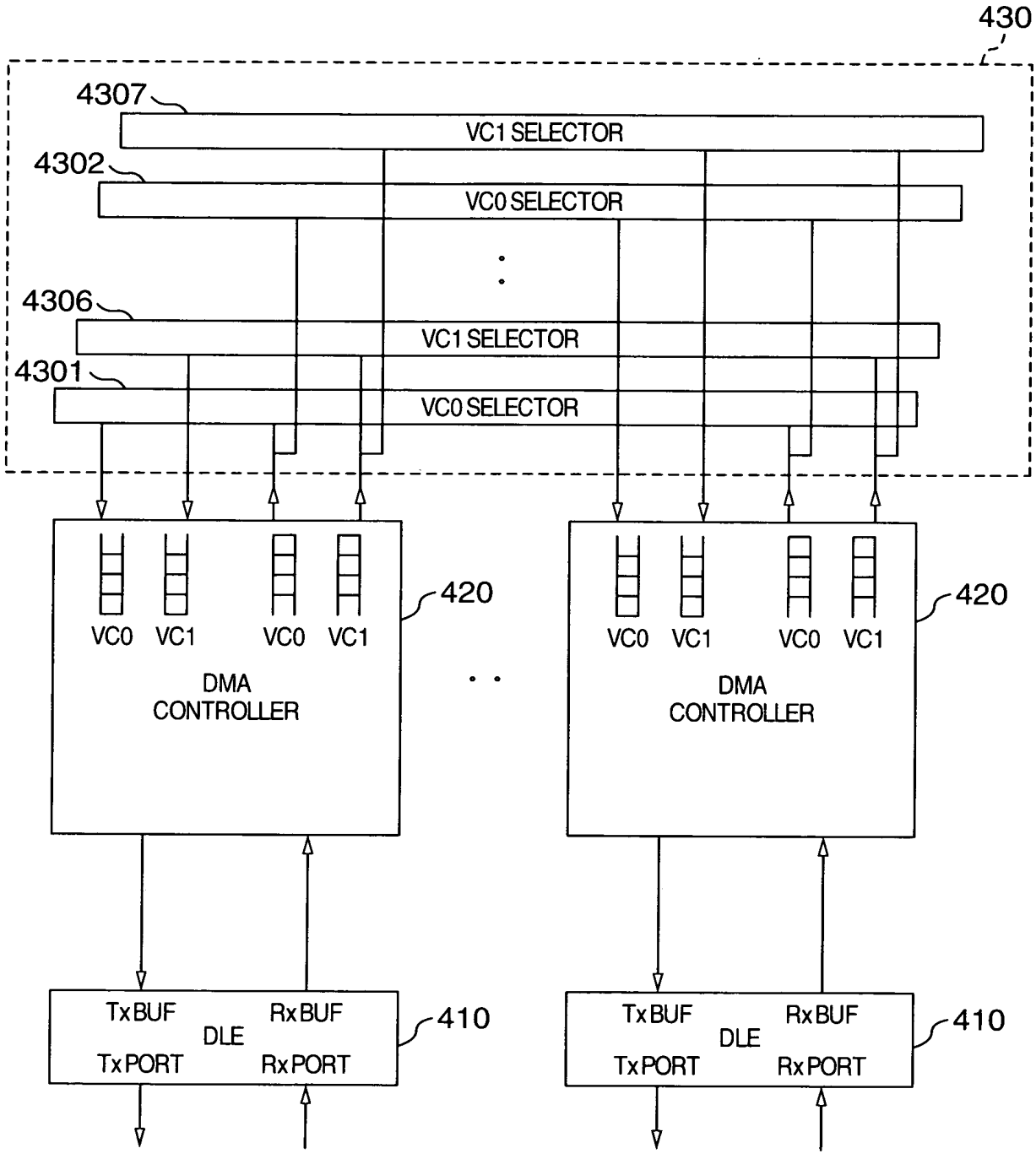

PROCESSOR ADAPTER STRUCTURE USED BY INVENTION

FIG. 6



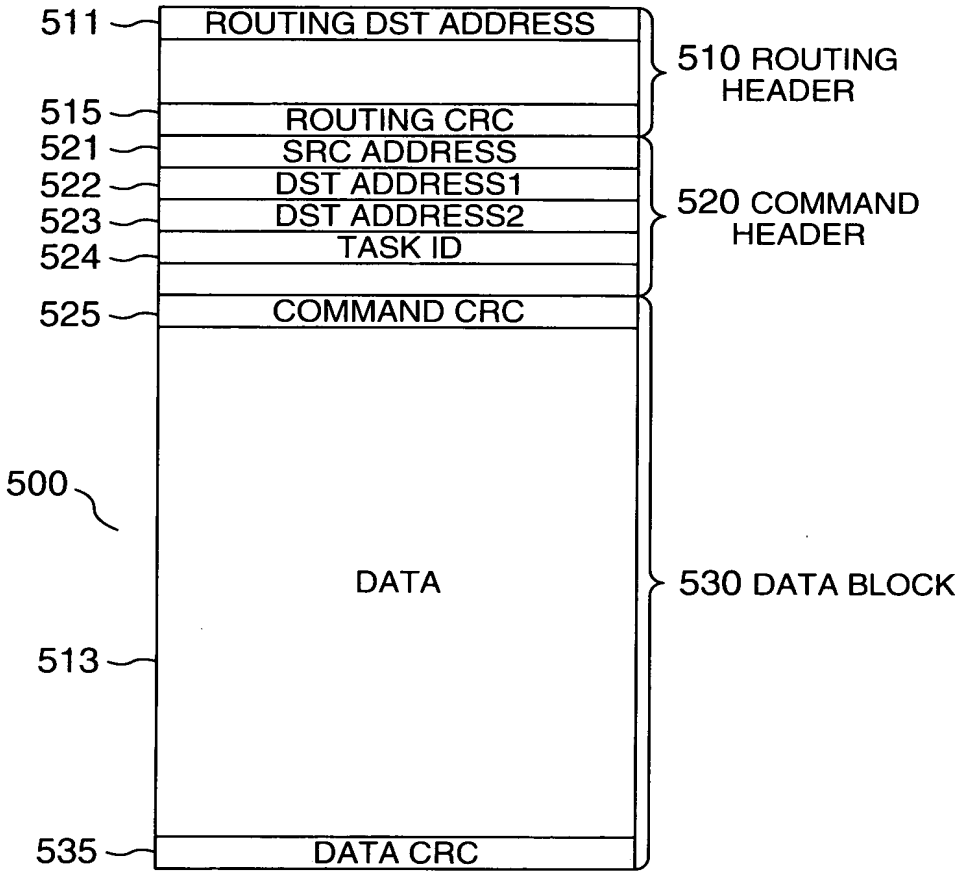

MEMORY ADAPTER STRUCTURE USED BY INVENTION

FIG. 7



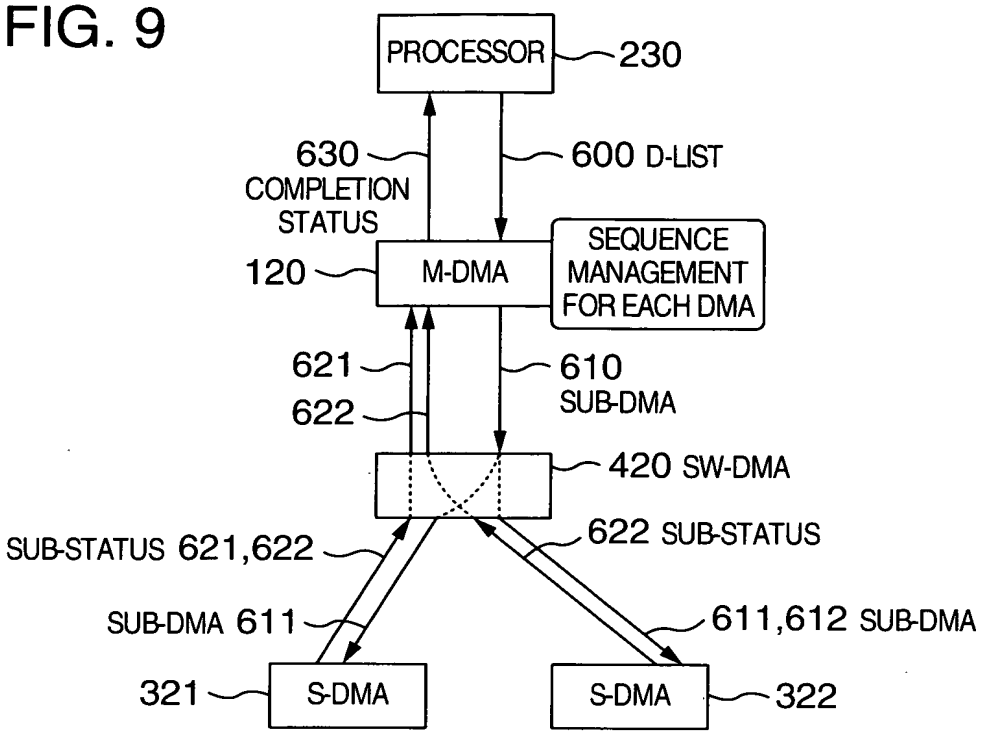

SWITCH ADAPTER STRUCTURE USED BY INVENTION

FIG. 8



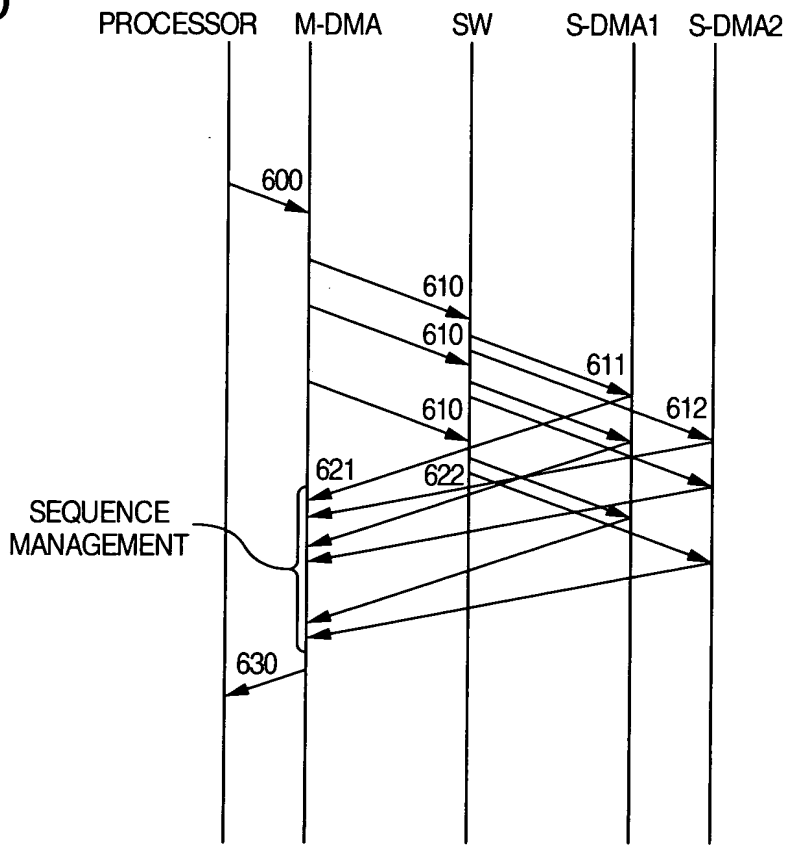

PACKET STRUCTURE USED BY INVENTION

FIG. 9



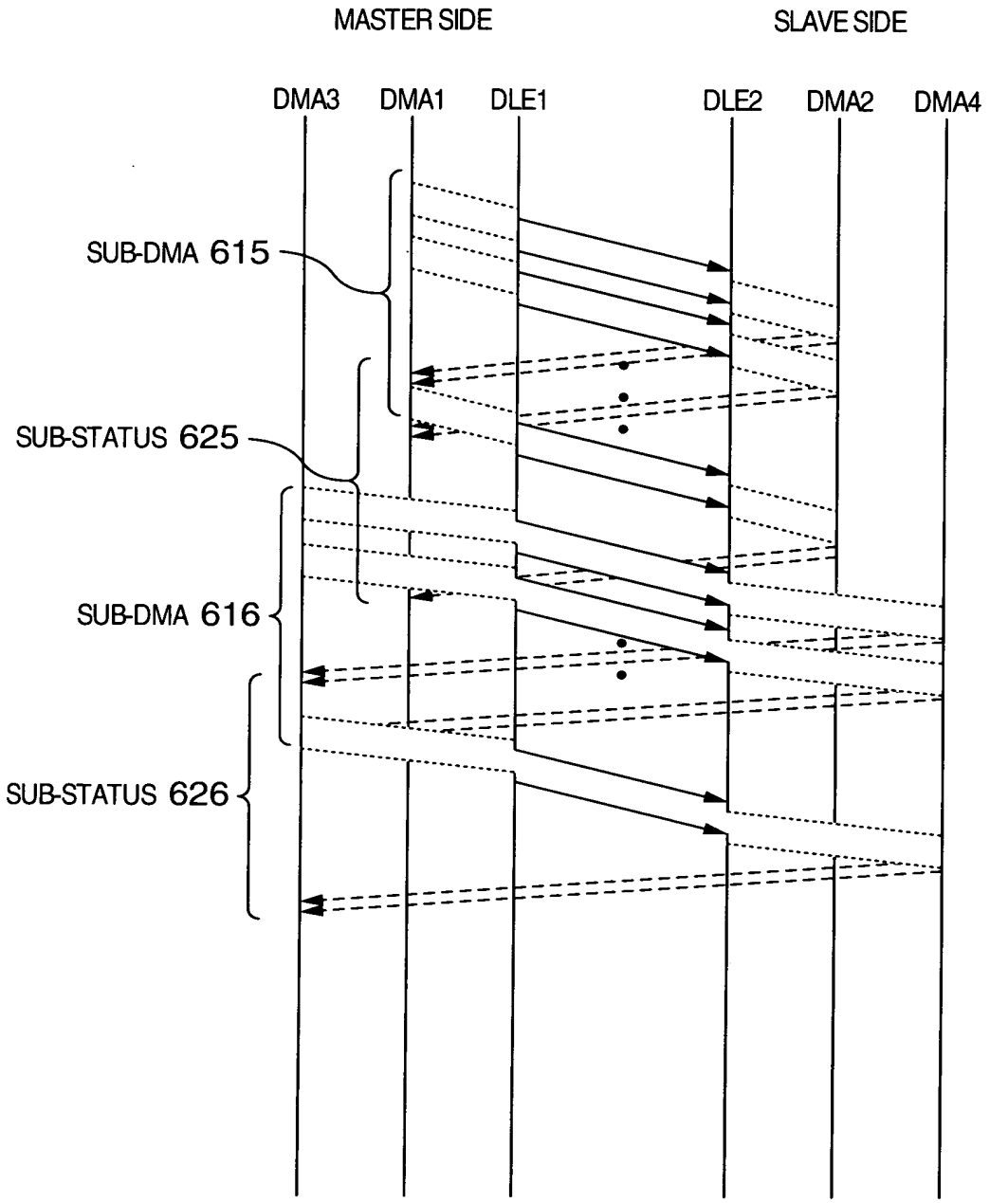

PACKET FLOW USED BY INVENTION

FIG. 10



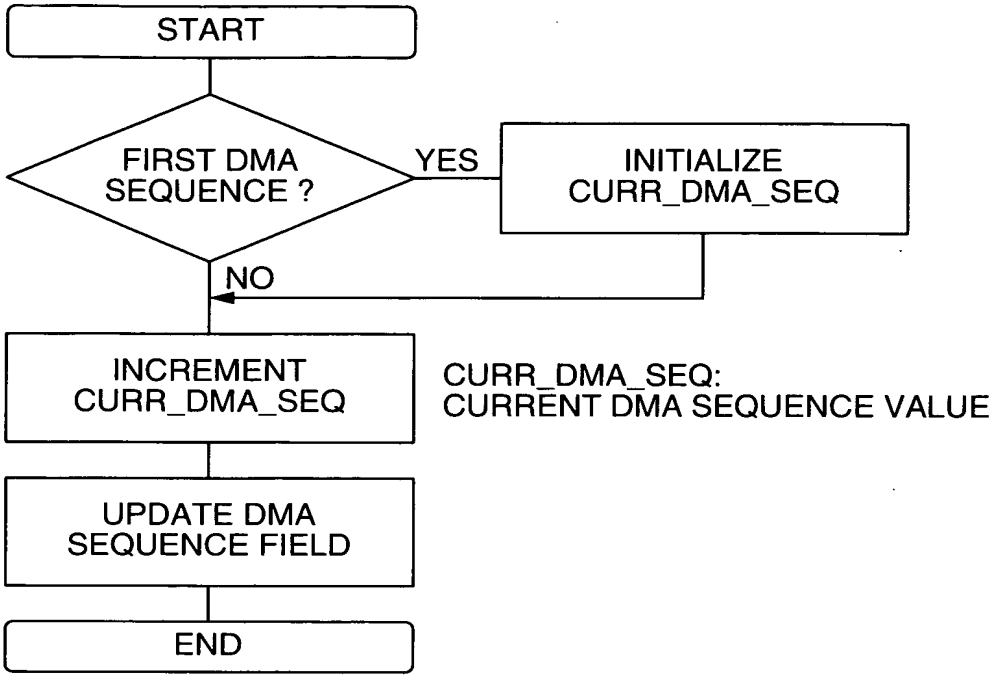

PROTOCOL USED BY INVENTION

# FIG. 11



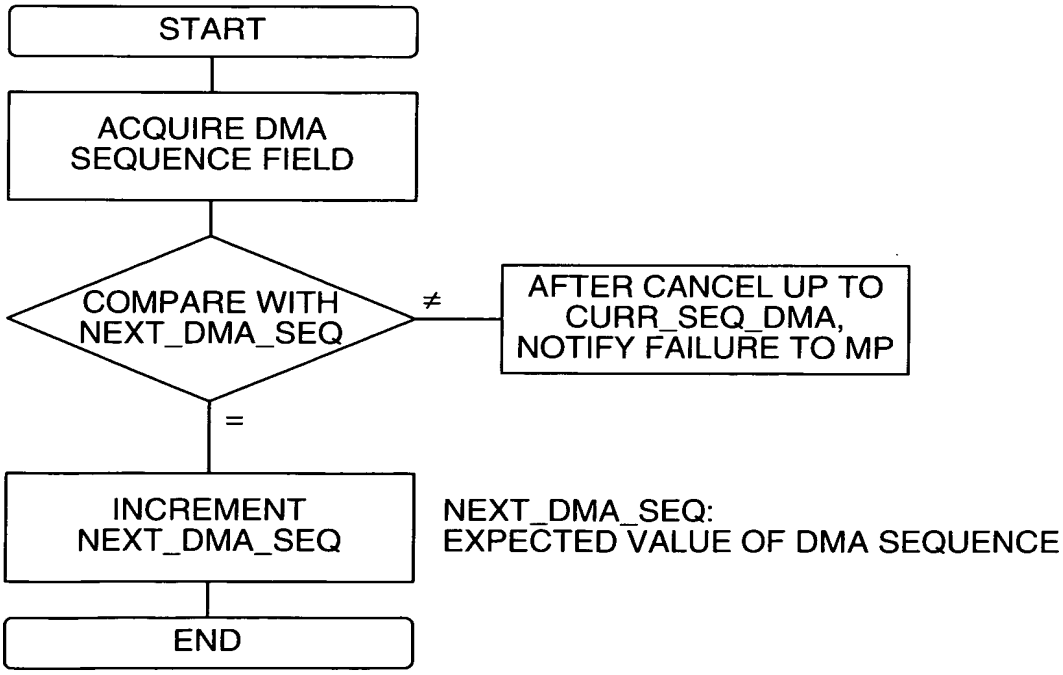

MULTIPLEX COMMUNICATION TRANSFER PROTOCOL

FIG. 12



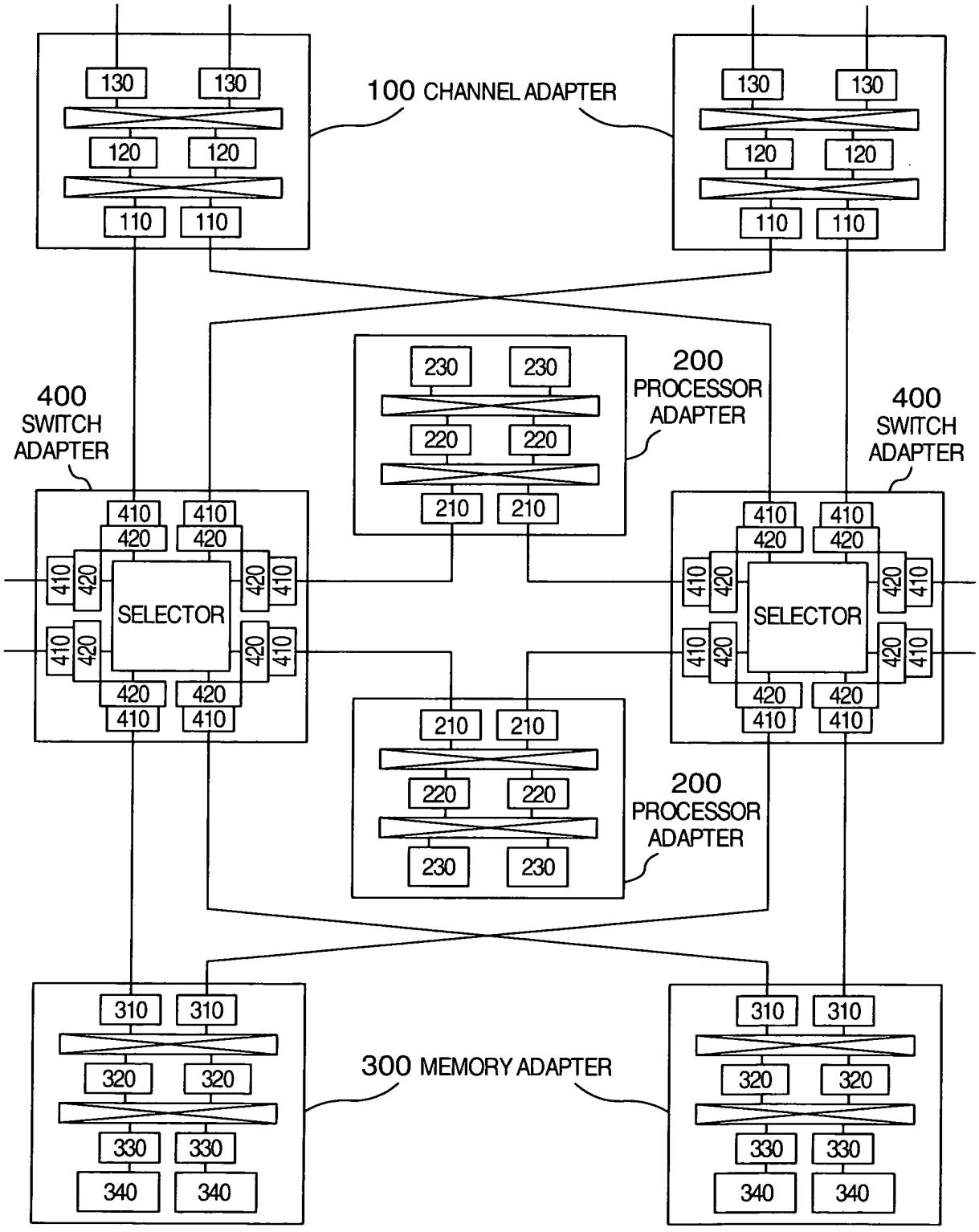

DMA SEQUENCE FIELD UPDATE FLOW DURING SUB-DMA TRANSMISSION

FIG. 13




DMA SEQUENCE FIELD CONFIRMATION FLOW DURING DMA SUB-STATUS RECEPTION

# FIG. 14




DISK CONTROLLER OF INVENTION

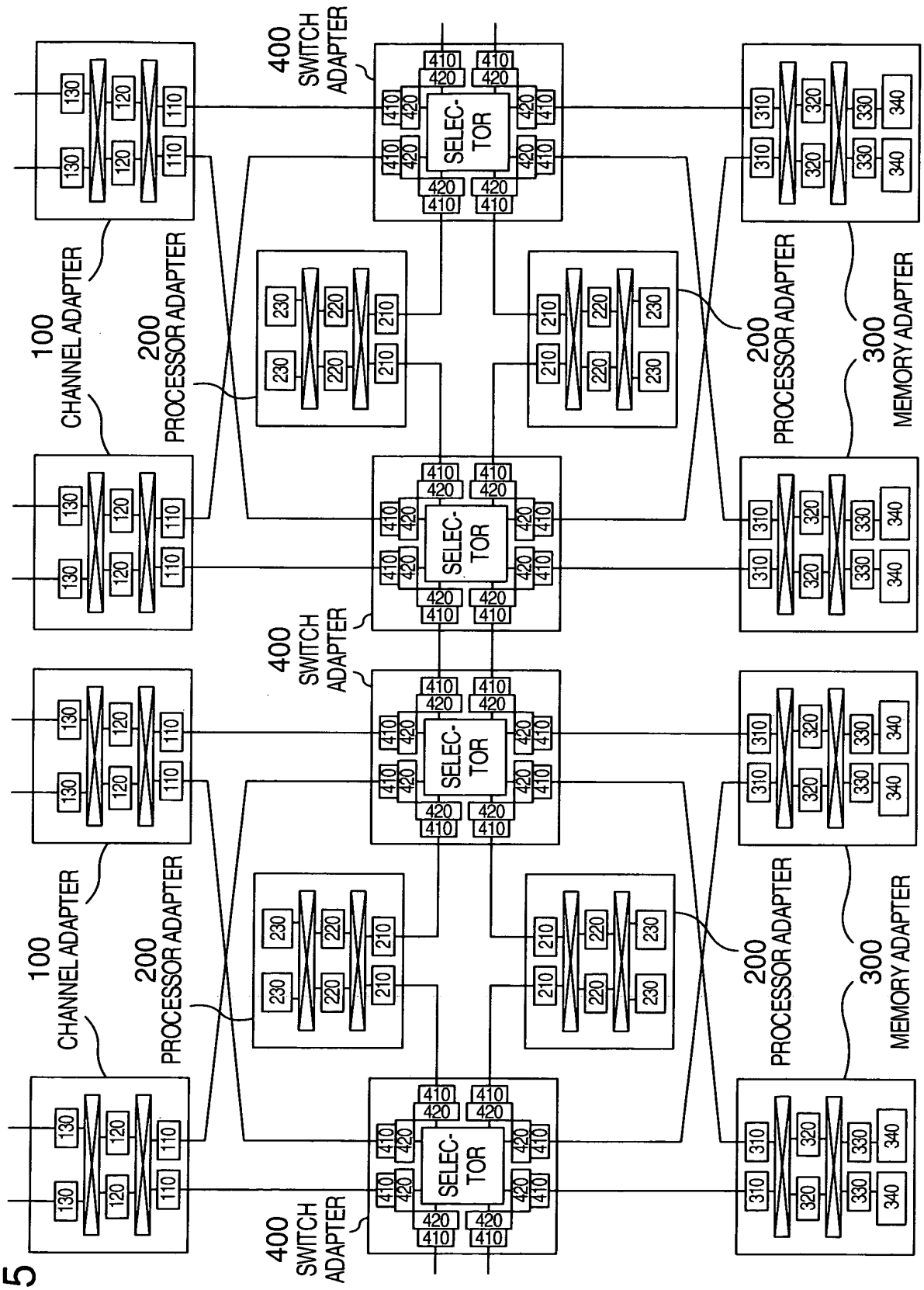
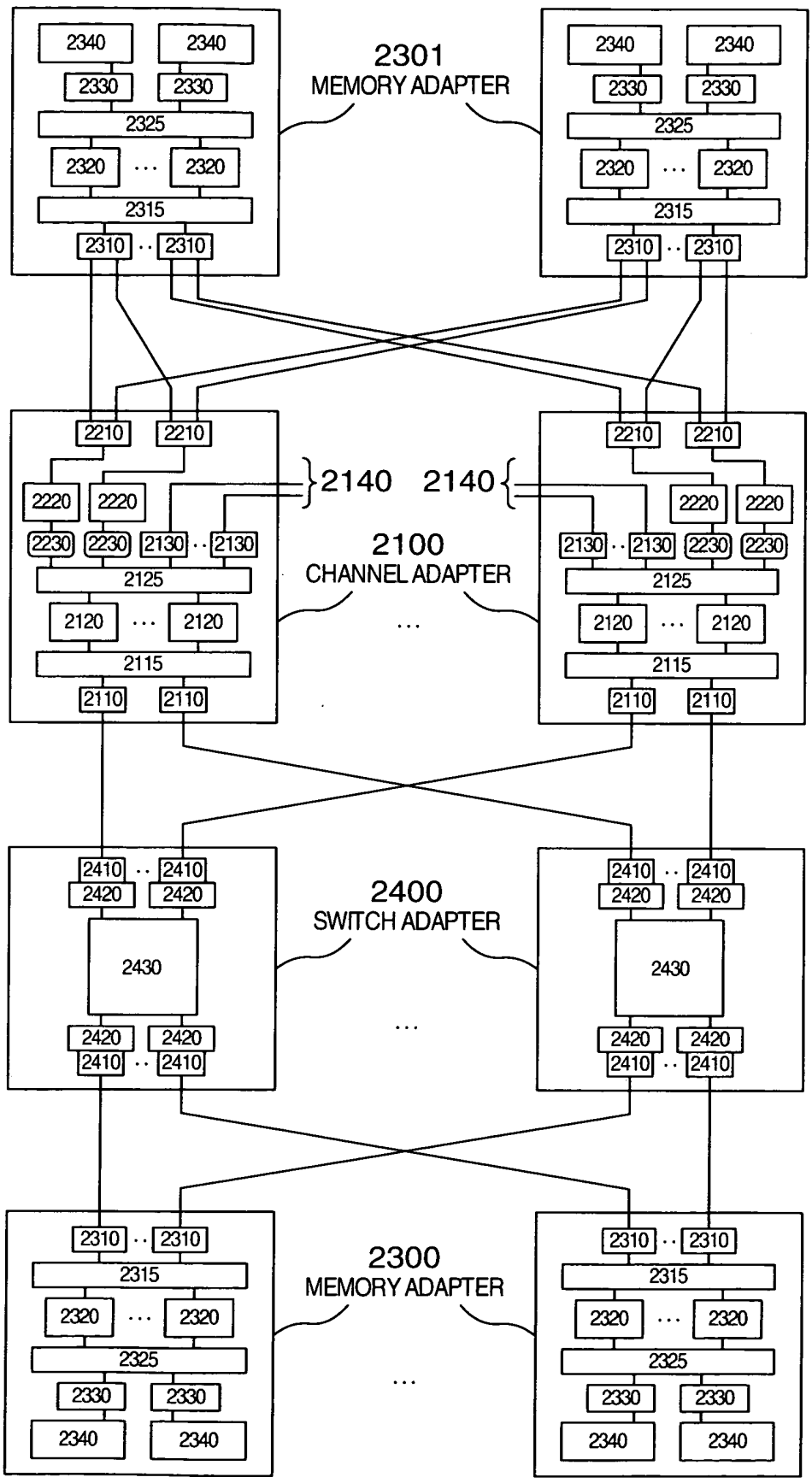

100
CHANNEL ADAPTER
200
PROCESSOR ADAPTER
400
SWITCH
ADAPTER
SELEC-
TOR
300
MEMORY ADAPTER
DISK CONTROLLER OF INVENTION

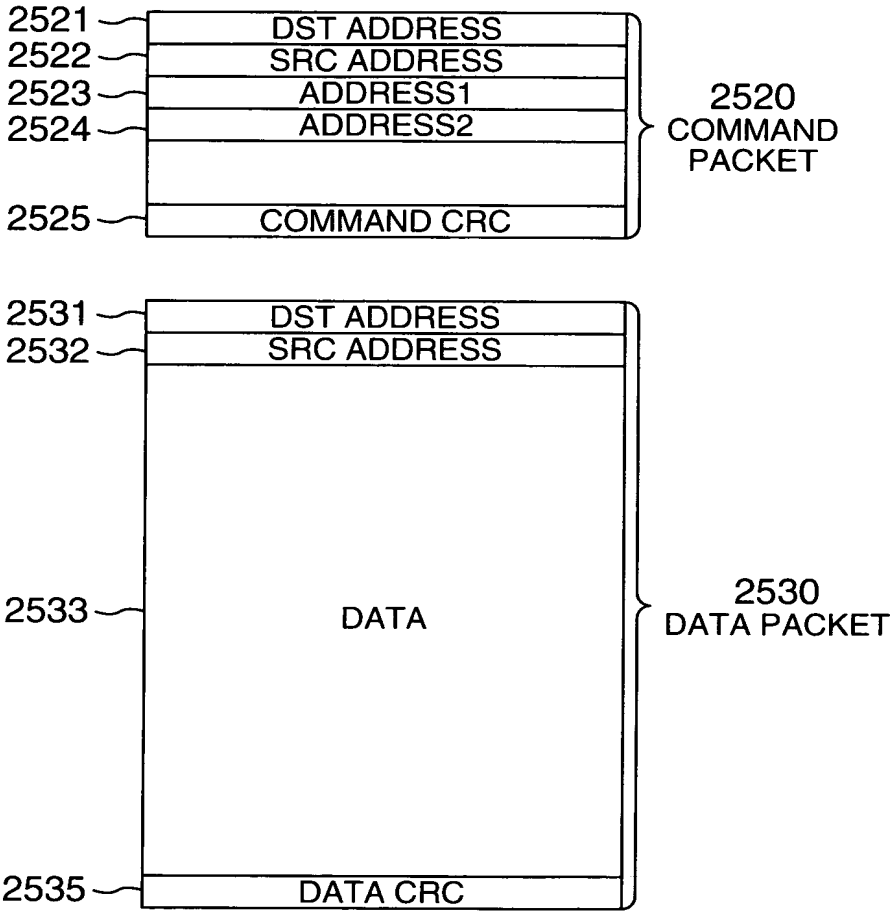
FIG. 15

FIG. 16



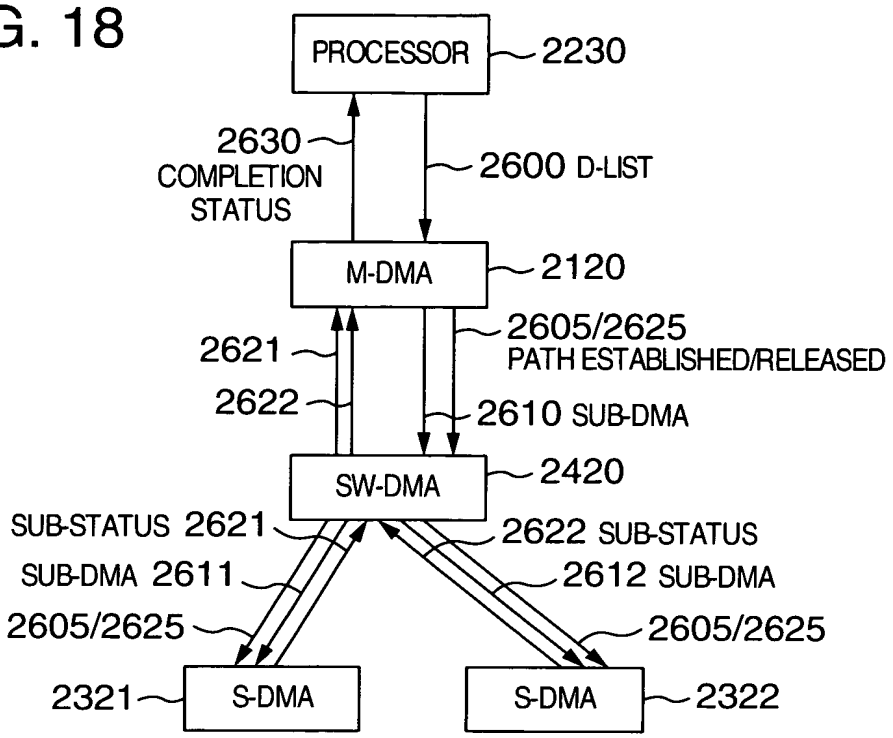

NETWORK CONFIGURATION OF CONVENTIONAL DISK CONTROLLER

FIG. 17



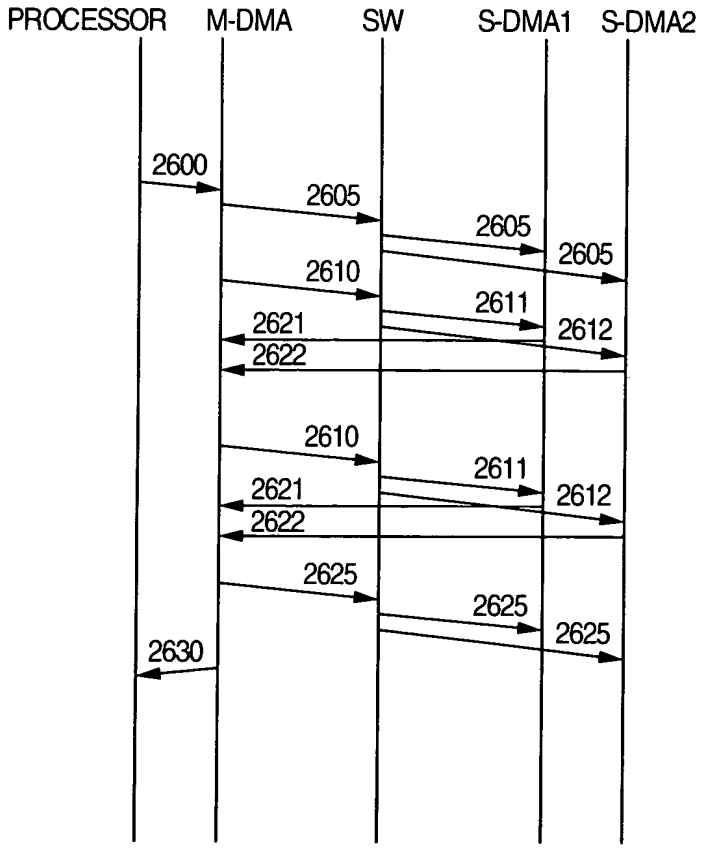

PACKET STRUCTURE USED BY CONNECTION TYPE COMMUNICATION SYSTEM

FIG. 18



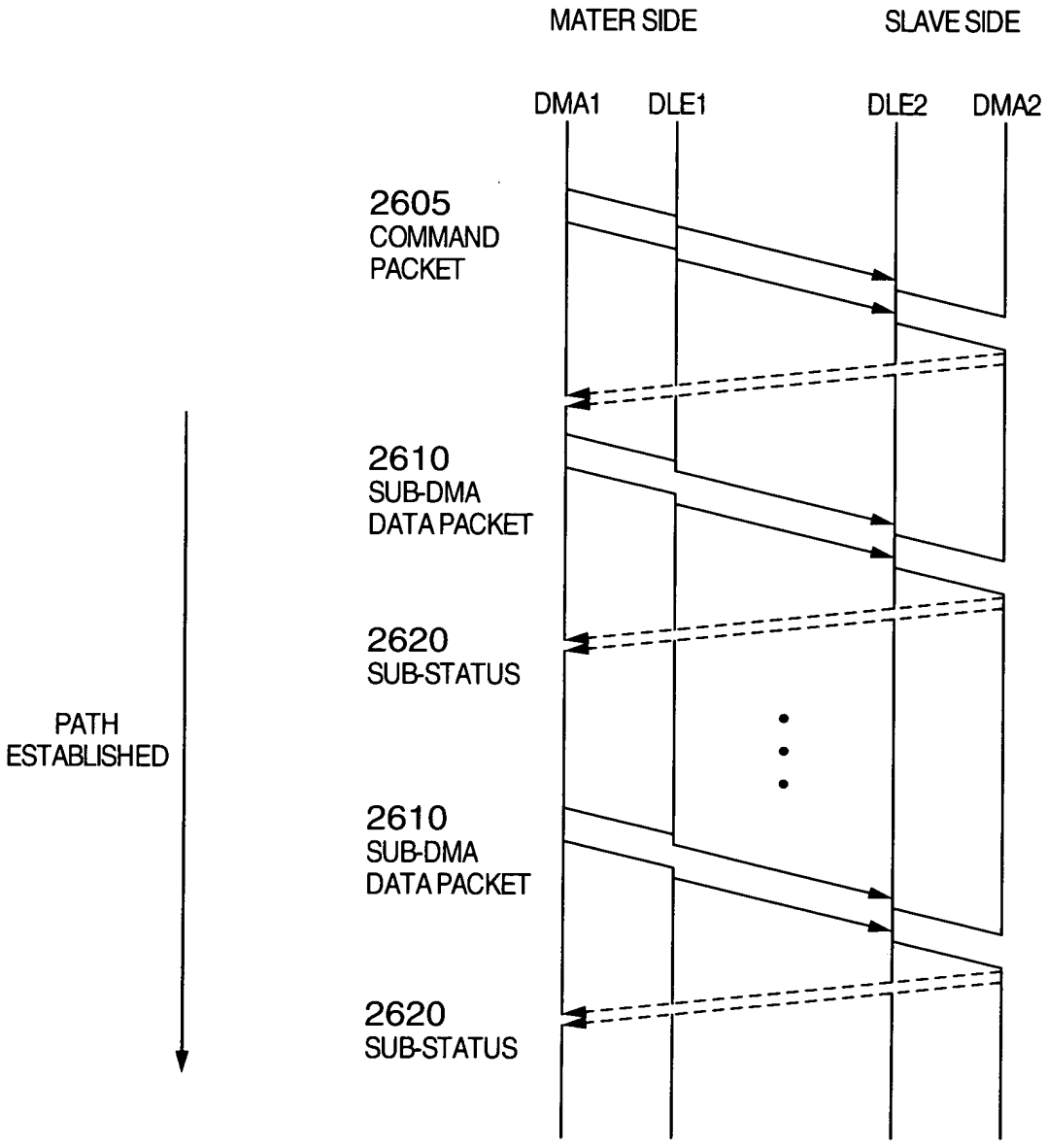

CONVENTIONAL PACKET FLOW

FIG. 19




CONVENTIONAL PROTOCOL

FIG. 20




NON-MULTIPLEX COMMUNICATION TRANSFER PROTOCOL